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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,241	10/22/2001	Kenneth A. Stewart	CS11493	4998

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,241	STEWART ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-10 and 14-17* is/are rejected.

7)☒ Claim(s) *5-7,11-13 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 31, 2005 has been entered.

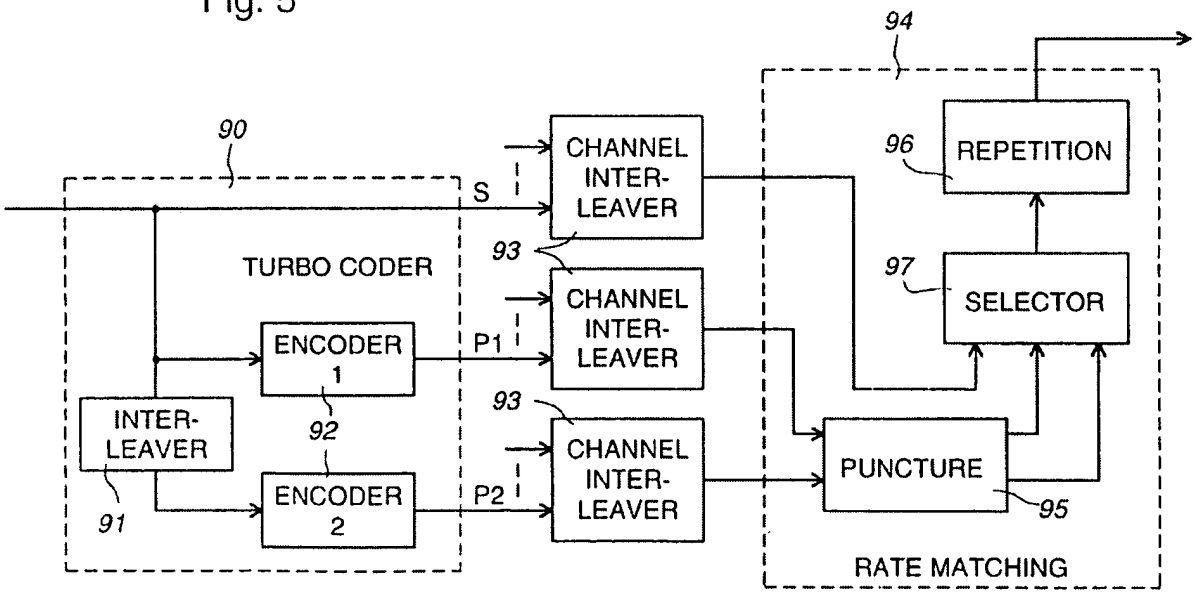
Response to Amendment

Applicant's arguments/amendments with respect to previously presented claims 1-20 filed October 31, 2005 have been fully considered but are not persuasive. Applicants are reminded claims 5-7, 11-13 and 18-20 remain objected to as being rejected from a base claim(s) and would be allowable in rewritten in independent form including the limitations of the base claim(s).

Applicant contends, "...Yamaguchi (prior art of record) fails to disclose selecting a predefined redundancy..." The Examiner respectfully disagrees. As stated in previous actions, the prior of are record, Tong teaches (Figure 5) a rate matching scheme wherein data bits in a matrix are interleaved by a predetermined interleaving process, to a desired rate by deletion of redundant data bits or repetition of data bits derived from the matrix. It includes steps of determining in a non-interleaved matrix of the data bits a pattern of bits to be deleted or repeated to provide the desired data rate, decoding an address of each bit in said pattern in a

manner inverse to the interleaving process to product a respective address of the bit in the matrix of interleaved data bits, and deleting or repeating the respective bit in the interleaved data bits in dependence upon the respective address. The address decoding is performed in the same manner as a coding of addresses for producing the interleaved data bits from the non-interleaved matrix of the data bits. The Examiner would like to point out that an encoder normally attaches a predefined amount of redundancy to data prior to transmission. Furthermore, a newly presented rejection under 35 USC 112 is given to independent claims with "predefined redundancy."

Fig. 5



The Examiner disagrees with the Applicant and maintains rejections/objections with respect to amended claims 5-7, 11-13, 17 and 18 and original claims 1-4, 8-10, 14-16, 19 and 20. All arguments have been considered. It is the Examiner's conclusion that claims 1-4, 8-10 and 14-17 are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1, 8 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "predefined redundancy" is indefinite because the adjective, "predefined" describing the noun, "redundancy" is a relative term. Meaning, the way that this term is used is in time order. In other words, the Examiner is not sure with respect to what is it predefined. Is it defined prior to transmission? Prior to encoding? Applicants are invited to clearly word claim language to overcome the prior arts of record.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4, 8-10 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (USPN 6480503B1) further in view of Tong et al. (USPN 6744744B1).

As per claims 1, 8 and 14, Yamaguchi et al. (herein after: Yamaguchi) substantially teaches (title and abstract) an encoder circuit (602) coupled to receive a data sequence. The encoder circuit produces a first encoded data sequence and a second encoded data sequence from the data sequence. A first spreading circuit (606) is coupled to receive the data sequence and the first encoded data sequence. The first spreading circuit produces a first modulated data sequence in response to a first code. A second spreading circuit (614) is coupled to receive the data sequence and the second encoded data sequence. The second spreading circuit produces a second modulated data sequence in response to a second code. In particular, Yamaguchi teaches (col. 3, line 50—col. 4, lines 39) an RSC encoder circuit receives the source sequence and produces parity bit sequences Y.sub.k.sup.1 and Y.sub.k.sup.2 at block 702. The source and parity sequences are divided into separate channels corresponding to blocks 704 and 706, respectively. One channel with sequences X.sub.k and Y.sub.k.sup.1 is modulated by circuit 710 with spreading code C.sub.A on lead 712. The other channel with sequences X.sub.k and Y.sub.k.sup.2 is modulated by circuit 714 with spreading code C.sub.B on lead 716. These data sequences are then transmitted to a remote receiver and demodulated by despreader circuits 718 and 724 with respective orthogonal spreading codes C.sub.A and C.sub.B on leads 720 and 724 as will be explained in detail. Data sequences from the separate channels are relayed to an RSC decoder 730 by blocks 726 and 728. The RSC decoder, shown in detail at FIG. 8, reproduce the source signal sequence at the receiver block 732. Referring now to FIG. 5, there is a block

diagram showing parity bit encoding by TMM corresponding to block 702. The encoder circuit is coupled to receive a data sequence D.sub.k on lead 100. This data is produced as output data sequence X.sub.k. The RSC encoder circuit 500 receives the data sequence and produces a first encoded data sequence Y.sub.k.sup.1 on lead 502 in response to a first code. An interleaver circuit 504 preferably stores the data sequence D.sub.k in an M.times.M matrix by rows and produces the data by columns on lead 506. A second RSC encoder circuit 508 receives the data sequence on lead 506 and produces a second encoded data sequence Y.sub.k.sup.2 on lead 510 in response to a second code.

Yamaguchi does not explicitly teach to select predefined redundancy as stated in the present application.

However, Tong et al. (herein after: Tong), in an analogous art substantially teaches to match the rate of data bits, in a matrix of data bits interleaved by a predetermined interleaving process, to a desired rate by deletion of redundant data bits or repetition of data bits derived from the matrix. It includes steps of determining in a non-interleaved matrix of the data bits a pattern of bits to be deleted or repeated to provide the desired data rate, decoding an address of each bit in said pattern in a manner inverse to the interleaving process to product a respective address of the bit in the matrix of interleaved data bits, and deleting or repeating the respective bit in the interleaved data bits in dependence upon the respective address. The address decoding is performed in the same manner as a coding of addresses for producing the interleaved data bits from the non-interleaved matrix of the data bits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the predefined redundancy of Tong with the method and apparatus of Yamaguchi. This modification would

have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by choosing to predetermine the amount of redundancy would optimize the encoding/decoding process as well as improve synchronization capabilities.

As per claims 2, 3, 9 and 15-16, Tong substantially teaches, in view of above rejections, (col. 3-4) after the functions 26 and 28, the resulting rate matched and interleaved signals are segmented for radio frames and physical channels in segmentation blocks 30 and 32 respectively to produce the signals for multiplexing by the multiplexer 10. Signals output by the multiplexer 10 are interleaved by a second interleaver 34 the outputs of which are segmented and mapped to dedicated physical channels in a segmentation and mapping block 36 for communications via a CDMA radio communications path in known manner. The first interleaver 28 can have a performance that is sufficiently good to enable the second interleaver 34 to be omitted or reduced to a simple shuffling operation. This is desirable in particular because the second interleaver 34 has the potential to degrade the interleaving performed by each first interleaver 28, whereas each first interleaver 28 can be optimized for its particular rate matched data stream and QoS. Accordingly, the first interleaver 28 is implemented as an algebraic interleaver providing a good random spreading property. The multiple encoded bit blocks or data transport frames for each QoS channel are mapped into a 2-dimensional matrix and are subjected to linear congruential rules to permute the rows and columns of the matrix to implement the interleaving function. A maximum interleaving depth and time span can be determined by searching a set of best parameters. The interleaver consequently has a relatively simple form without disadvantages of known interleavers, such as requiring large memory sizes for look-up tables or inadequately accommodating the rate matching function.

As per claims 4, 10 and 17, Tong substantially teaches, in view of above rejections, that the rows and columns can be interchanged without changing the function of the interleaver, and that in practice and as described below the interleaver can operate by equivalent control of read or write addressing of memory locations of a linear memory in which data bits are stored, without any actual movement of the stored bits among the memory locations.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
December 26, 2005

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